UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,348	12/11/2003	Chang-Cheng Yap	60430 (71987)	3764

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EXAMINER
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ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 December 2003_.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-17_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-17_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _11 December 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   This Office Action is responsive to the Application filed on December 11, 2003.

Claims 1-17 are presented for examination. The Foreign Priority Date as of December

26, 2002 has been considered.

Claims 1-17 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Krueger

et al. (US Patent 6,173,368).

As per claims 1 and 12, Krueger et al. disclosed a method and system for

accessing memory data, for providing a data storage buffer mechanism for a non-

cacheable memory region in a memory unit of an electronic device (See Fig. 3 and

claim 1), the method comprising the steps of:

having an interface unit receive a memory accessing request from a processing

unit, and allowing a non-cacheable memory buffer unit to conduct a comparison to

determine if there is a memory address corresponding to that in the memory accessing

request, if no, forwarding the memory accessing request to an arbitration unit for

accessing data in the memory unit (See claim 1, lines 52-60, and claim 23, wherein Krueger et al. disclosed a method of comparing the accessing memory address with the stored address in the non-cacheable memory buffer and retrieve the matched data else access the data from the external memory if it is a miss);

having the non-cacheable memory buffer unit retrieve memory data during transmitting the data from the memory unit to the interface unit to update data stored in the non-cacheable memory buffer unit (See claim 2, col. 27, wherein the non-cacheable data storage circuit is being modified after a new data has been stored);

having the non-cacheable memory buffer unit pre-read continuous memory address data following the retrieved data to enhance speed of accessing the continuous data for the processing unit (See claim 8, pre-fetch).

As per claim 2, Krueger et al. disclosed the method of claim 1, wherein the memory data is read when there is a memory address corresponding to that in the memory accessing request (See claim 23, lines 55-57).

As per claims 3 and 13, Krueger et al. disclosed the method and the system, wherein the electronic device is selected from the group consisting of personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.   See col. 2, lines 1-10, wherein the Krueger et al. disclosed microprocessor-based systems which included personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.

As per claims 4 and 14, Krueger et al. disclosed the method and the system, wherein the memory unit is selected from the group consisting of static random access memory, dynamic random access memory, synchronous dynamic random access memory, and high-speed data-transmission synchronous dynamic random access memory. See col. 1 line, 40 – col. 2, line 30.

As per claims 5 and 15, Krueger et al. disclosed the method and the system, wherein the processing unit is a central processing unit or microprocessor. See col. 1, lines 35-37.

As per claim 6, Krueger et al. disclosed a method for accessing memory data, for providing a data storage buffer mechanism for a non-cacheable memory region in a memory unit of an electronic device (see Fig. 3 and claim 1), the method comprising the steps of:

when a processing unit, apparatus or module of the electronic device writes data to the memory unit, having a non-cacheable memory buffer unit compare if a memory address of the written data is consistent with that of data stored in the processing unit, apparatus or module of the electronic device (See claims 2 and 3, wherein the processor comparing the data consistency with the non-cacheable storage unit (claim 2) before writing to external memory (claim 3); and

when the consistency of memory address is verified, having the non-cacheable memory buffer unit update the data of the consistent memory address (See claim 3).

As per claim 7, Krueger et al. disclosed the method of claim 6, wherein the electronic device is selected from the group consisting of personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation. See col. 2, lines 1-10, wherein the Krueger et al. disclosed microprocessor-based systems which included personal computer, notebook computer, palm computer, personal digital assistant, server, and workstation.

As per claim 8, Krueger et al. disclosed the method of claim 6, wherein the memory unit is selected from the group consisting of static random access memory, dynamic random access memory, synchronous dynamic random access memory, and high-speed data-transmission synchronous dynamic random access memory. See col. 1 line, 40 – col. 2, line 30.

As per claim 9, Krueger et al. disclosed the method of claim 6, wherein the processing unit is a central processing unit or microprocessor. See col. 1, lines 35-37.

As to claims 10, 11, 16, and 17, the applicant's claim invention is relating to the processor-based systems. Therefore, an electronic device that is an external peripheral device or embedded peripheral device is well known and use concurrently with any of the processor-based systems.

Therefore, claims 10, 11, 16, and 17 are rejected under the same rationale.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
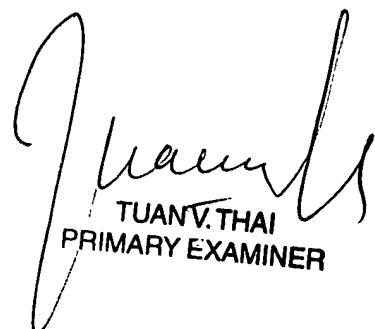
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh D. Vo

Patent Examiner

12/27/2005

TUAN V. THAI
PRIMARY EXAMINER